AMENDMENT TO THE SPECIFICATION

Please amend the specification as follows:

[0008] However, in the inverter driver according to the conventional duty control method, the current waveform of the CCFL is steeply varied when the duty greatly reduces or increases~~, and~~. Accordingly, the brightness of the CCFL becomes unstable, interference occurs in the adjacent circuit because of many harmonics thereof, and the lifetime of the CCFL shortens.

[0021] FIG. 1 shows an inverter driver according to a first preferred embodiment of the present invention~~;~~.

[0022] FIG. 2 shows a ratio of a voltage V1 versus a voltage V2, and a relation between a voltage Vct and a frequency f in the inverter circuit ~~100;~~.

[0023] FIG. 3 shows a signal waveform diagram according to a first preferred embodiment of the present invention~~; and~~.

[0029] The inverter circuit 100 uses a serial/parallel resonance of a half bridge inverter~~; and a~~. A resonance frequency of the inverter circuit 100 is a frequency whereby the total impedance of the inductor L1 and the capacitors C1, C2, and C3 becomes zero in the viewpoint ~~of~~ from the primary side to the secondary side ~~of~~ the inverter circuit 100.

[0030] Body diodes D1 and D2 are respectively coupled to the switches M1 and M2 of the inverter circuit 100~~, and the~~. The body diodes enable zero voltage switching of the switches M1 and M2 as described later.

[0031] The control signal supply 200 comprises resistors R1 and R2 coupled in series between the input voltage Vcc and ground~~; a~~. A subtractor 220 ~~for~~ subtract~~ings~~ a voltage Vnc at a node between the resistors R1 and R2 from a reference voltage Vr and outputting a subtraction voltage Va (Va=Vr-Vnc)~~; a~~. A comparator 240 ~~for~~ compar~~inges~~ a reference

voltage Vref and a feedback voltage Vfb at a resistor Rsense sensing the current flowing to the CCFL 10, amplif~~ying~~ies the comparison result, and output~~tings~~ a voltage Vcomp~~; and a~~. A multiplier 260 ~~for~~ multipl~~ying~~ies output signals of the subtractor 220 and the comparator 240 by a predetermined gain K to generate a voltage Vmo, and supply~~ing~~ies the voltage Vmo to the duty controller 300.

[0034] The comparator 310 compares the output voltage Vmo of the control signal supply 200 with a voltage Vct charged in the capacitor Ct of the frequency controller 400, and provides a comparison result to the R ~~end~~ terminal of the RS latch 320. The S ~~end~~ terminal of the RS latch 320 receives clock signals CLK from an oscillator 410 of the frequency controller 400. Signals output from the Q' ~~end~~ terminal of the RS latch 320 and the clock signals CLK of the oscillator 410 are input to two input ~~ends~~ terminals of the OR/NOR logic gate 330. Two output signals of the OR/NOR logic gate 330 are respectively provided to the high-side gate driver 350 for driving the switch M1 and the low-side gate driver 340 for driving the switch M2.

[0038] When the voltage Vt obtained by subtracting the voltage Vx from the voltage Vcomp is greater than the voltage Vrt, the current IC1 flows to the resistor Rf, and the current ICt which is the difference ~~IC2-IC1~~ between the currents IC1 and IC2 (i.e., IC2-IC1) flows to a terminal of the oscillator 410 to which the resistor Rt is coupled.

[0039] The capacitor Ct is coupled to the oscillator 410~~, and since~~. Since the current flowing to the capacitor Ct is matched with the current ICt, the current ICt charges or discharges the voltage at the capacitor Ct.

[0041] Given an amplitude V of the voltage Vct, the period of the voltage Vct charged in the capacitor Ct is the summation of the charge time (CtxV)/ICt and the discharge time (CtxV)/ICt~~, and accordingly~~. Accordingly, the frequency f of the voltage Vct is given as Equation 2.

[0046] The operation frequency region of the inverter driver is between the minimum

frequency f_{low} and the maximum frequency f_{high}~~, and as~~. As given in Equation 2, since the capacitor Ct is constant and the amplitude V of the voltage Vct is also constant, the maximum frequency f_{high} is obtained when the current ICt is a maximum, and the minimum frequency f_{low} is obtained when the current ICt is a minimum.

[0047] Since ICt=IC2-IC1 and IC2=Vrt/Rt, the ICt becomes the maximum and the frequency of the voltage Vct accordingly becomes the maximum frequency f_{high} when IC1=0~~, and~~. ICt becomes the minimum and the frequency of the voltage Vdt becomes the minimum frequency f_{low} when IC1 is the maximum.

[0069] The output voltage Vcomp of the comparator 240 is input to ~~a non~~ an inverting end of the OP amp 430, and a resistor Rf is coupled between an inverting end of the OP amp 430 and the ground voltage. Since the voltages at the inverting and non-inverting ends of the OP amp 430 are the same, the voltage Vcomp is applied to both ends of the resistor Rf, and the current IC1 flowing to the resistor Rf is Vcomp/Rf.